

Modeling of Inductors and Transformers

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Abstract — This paper deals with modeling of spiral inductors and transformers. A lumped element approach is used to represent the spirals on a turn-by-turn basis. A previously reported approach for modeling of substrate eddy currents is employed and a new approach for modeling of current crowding effects is introduced. Both are modeled using inductor and resistance loops with coupling to the turn inductances. The program is written to generate a spice sub-circuit for a wide variety of inductors and transformers. The results are validated against measured values of spirals implemented in a six-layer-copper bulk CMOS process and an SOI process.

I. INTRODUCTION

Integration of active components needed in wireless products is well understood, whereas, integration of passives is still a challenging endeavor. Passives such as inductors and transformers on a chip form the core to a successful integrated transmitter or receiver. The values of inductance (L), quality factor (Q) and self-resonant frequency (SRF) are critical to a good design. Unfortunately there are no simple formulas to determine them accurately and we enter the realm of simulations and modeling to determine these parameters. Although there are products in the market which do electromagnetic simulations to determine these parameters, they are computationally expensive and often have problems of convergence in multi-layered spirals. The program described in this paper calculates the different parameters using a lumped element approach for single and multi-layered spirals and has been found to produce accurate results. A public domain version of this program is made available for general use [7].

II. MODEL OVERVIEW

The spiral is broken on a turn-by-turn basis for each layer. A series inductance and resistance represent the spiral for a turn. As shown in Fig. 1b, the capacitance to the substrate from the lowest layer is represented on either side of the turn. The epi resistance connecting between the capacitor bottom plates is shown by R_{epi} . As there is also a parallel path between the two ends of the turn through the substrate, it is represented by the

resistance R_{sub} . The simplified model for a single turn is shown in Fig. 1b. The Resistance R_{s1} is the epi resistance connecting the substrate through the epi layer. This model is an extension and modification of the models published previously [2,3,8].

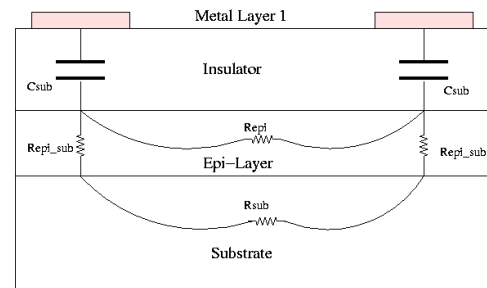


Figure 1a: Simplified model of an IC showing the different resistances

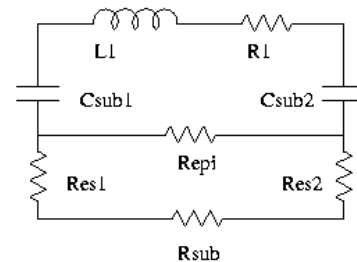


Figure 1b: Model for a single turn

III. MODEL DETAILS

A three-turn, two-layered spiral is discussed with the calculation of the different parameters. Fig. 2 shows the top view of a three-turn spiral with the different parameters needed to specify its dimensions. As shown in Fig. 4, the models for the individual turns are connected in series to give the complete model. The turns of layer 2 are shielded from the substrate and they only have interlayer capacitance to the adjacent layers. The interlayer capacitance is shown in Fig. 3 and can be calculated by the standard parallel plate capacitance.

$$C_{sub} = \epsilon_0 \epsilon_r l w / d \quad (1)$$

Where l is the length and w the width of the trace and d is the distance between the layers.

Fig.3 also shows the side-wall capacitance between the adjacent turns. It can also be calculated using equation (1) neglecting the fringing effects.

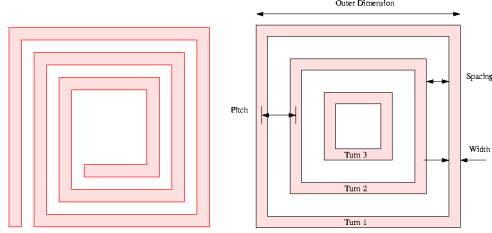


Figure 2: Illustration of geometry of a spiral and closed turn approximation used in this program

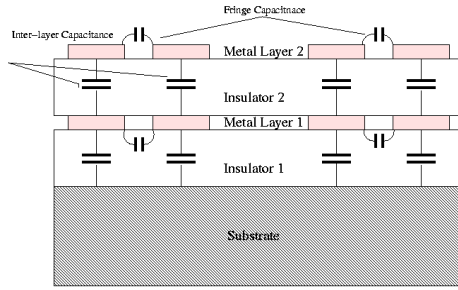


Figure 3: Illustration of different capacitances in a stacked-two-layer spiral

The coupling coefficients between the different self-inductances are calculated by finding the B field inside the spiral. It is seen from Fig. 4 that the coupling between L1 and L2 is the same as between L1 and L5, assuming the whole of flux linking L2 also couples through L5.

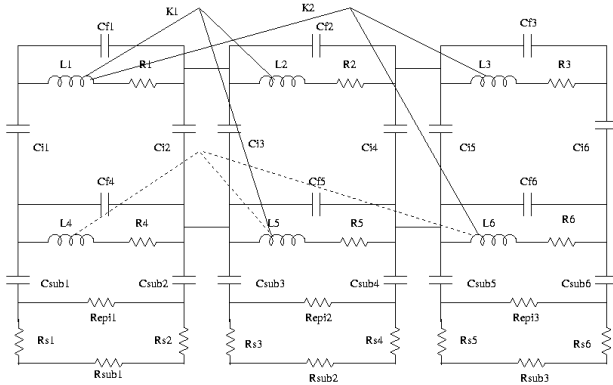


Figure 4: Lumped Model showing a two-layer, three turn spiral without a ground shield (all the coupling coefficients are not shown)

IV. PATTERNED GROUND SHIELD MODEL

In medium resistivity substrates, currents flowing through the substrate resistances discussed above are

major degrader of Q of the spiral [4-6]. Hence a low resistance path should be provided for the displacement current using a shield or a ground plane. The ground plane is made using the lowest metal layer or a poly layer, which is patterned to prevent an eddy loops in it. The modified model of Fig. 4 could then be represented by Fig. 5. It can be seen that the turn-to-substrate capacitances are now connected through the low valued shield resistances R_{s1} , R_{s2} and R_{s3} . The rest of the parameters remain the same.

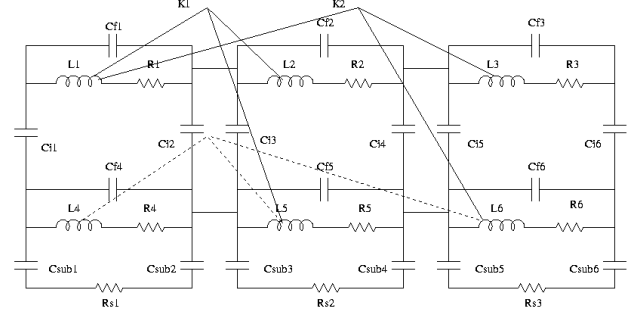


Figure 5: Lumped Model showing a two-layer, three turn spiral with a ground shield (all the coupling coefficients are not shown)

V. EDDY CURRENT LOSSES

There are two kinds of eddy currents losses that degrade the Q of the spiral, eddy currents in the substrate formed by the magnetic coupling from the traces and current crowding in the traces of the spiral.

In typical CMOS IC processes, the underlying substrate contributes losses to the Q of the spiral due to the large currents induced in the low resistivity bulk under the epi layer [3]. A simplified lumped element approach is used to model these effects and thus enable us to incorporate the effects into a spice sub circuit model. The excitation current in the traces generate a magnetic field, which creates eddy loops in the substrate [3]. This can be modeled by inductance resistance loops and coupled to the main turns inductances by coupling coefficients. The inductance values are the same as the self-inductances of the main turns whereas the resistances will be calculated based on estimate of the area of the substrate where the currents are significant. It can be calculated

$$R_{sub} \approx 6 \rho l / w D \quad (2)$$

Where ρ is the resistivity of the substrate, D the outer dimension of the spiral.

Fig.6 shows the modeling for eddy losses for each turn of the spiral. The coupling coefficients between a turn in the spiral and an eddy loop directly below it are approximated to be equal to 1, while other K values are estimated in the same way as between the turn

inductances. The coupling coefficient K_2 in Fig. 4 would be the same as K_2 in Fig. 6, assuming the distance between the layers is small compared to the distance between the turns. In the case of Lddy1, there is a coupling from all the main turn inductors given by coupling coefficients K_1 , K_2 and K_3 .

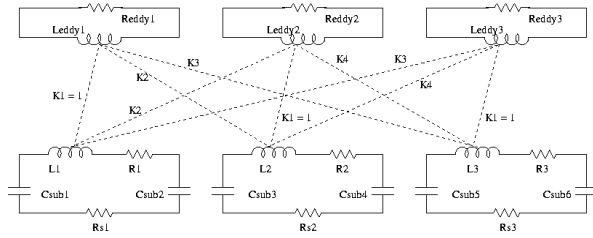


Figure 6: Eddy current modeling for a one-layer, three-turn spiral showing the coupling coefficients between the different inductors

VI. MODELING CURRENT CROWDING EFFECTS

In multi-turn spirals current crowding causes the effective series resistance to increase at higher frequencies [1,4-6]. Fig. 7 shows the general effect of current crowding on Q and R of the spirals [2].

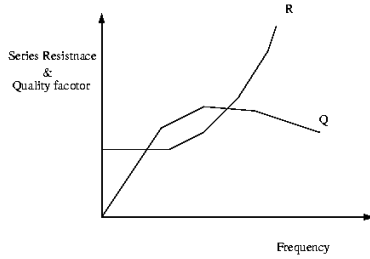


Figure 7: Graph showing the general effect of current crowding on Resistance and Q

Eddy currents are produced in the traces because of the B field of the adjacent turns, penetrating normal to the surface as illustrated in Fig 8. This current adds to the excitation current in the inside edges and subtracts from the outside edges.

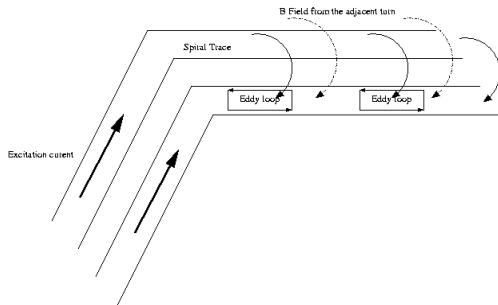


Figure 8: Eddy loops formed on the traces due to magnetic field generated by the adjacent turns.

At lower frequencies the crowding current is in quadrature and the power losses contributed by it can be added directly to the losses contributed by the excitation current [1]. This can be modeled using inductor resistor loops with coupling coefficients connecting to the turn inductances.

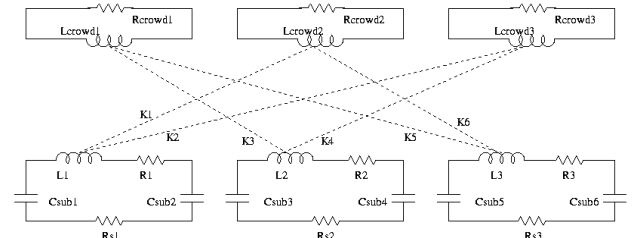


Figure 9: Eddy current modeling for a one-layer, three-turn spiral showing the coupling coefficients between the different inductors

The inductance of current crowding loop can be estimated using the formula for two-wire transmission line with cylindrical conductors [1].

$$L_{\text{eddy}} \approx \mu_0 L \ln(W / W/4) / \pi \quad (2)$$

Where L and W are length and width of traces.

Resistances can be estimated by assuming the current in 25 % of the trace width and thus R_{crowd} would be [1]

$$R_{\text{crowd}} \approx 2 R_{\text{sheet}} L / W/4 \quad (3)$$

The important part is determining the coupling coefficients between the different inductors. As discussed in earlier section, the B field generated by each turn is used to determine the coupling between the series inductors and the current crowding inductors. As can be seen from Fig. 9 there is coupling only to current crowd inductors from other turns.

VII. SPIRAL GEOMETRY OPTIONS

The different types of spirals modeled in this work are listed below.

- Single and multi-layer inductors
- Stacked transformer, with primary in one layer and the secondary in another layer.
- Interwound transformer, with primary and secondary on the same layer.
- Stacked-Interwound,, with primary and secondary turns equally divided between two layers. It is the combination of stacked and interwound type transformer and has the best of both.

Fig. 10 shows the complete model for a multi-layered spiral after all the loss mechanisms are taken into effect.

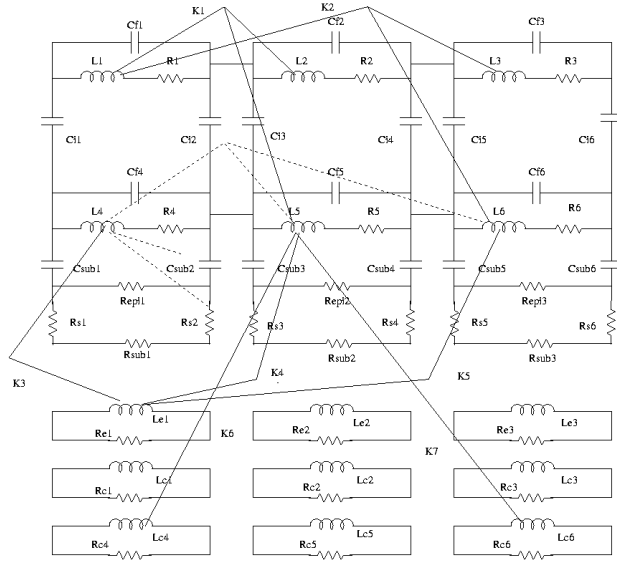


Figure 10: complete model of a two-layer, three turn spiral(all coupling coefficients not shown)

VIII. VALIDATIONS AGAINST MEASURED RESULTS

These models were validated against measured values from inductors and transformers under different processes. The inductors were validated in a six-layer-copper bulk CMOS process and in an silicon-on-sapphire (SOS) process. The validations indicate that the quality factor (Q) and inductance (L) are typically within 10% of measured value whereas the self-resonant frequency (SRF) varied 10 – 20 % depending on the absence or presence of ground shield. The results are tabulated in the table below with the first three cases in copper process and the last in SOS.

Case	L(nH)		R(Ω)		Q@1.2Ghz		SRF	
500x2x50	3	3.6	1.3	1.3	6.7	7.8	4.8	3.7
500x2x50 *	3	3.6	1.5	1.3	7.6	8.3	2.7	3.1
500x3x50 *	5.1	6.4	1.8	1.9	7	8.5	1.7	1.9
350x6x18	9.4	10.2	8.7	8.6	7.3	7.7	2.9	3.1

Table 1: Simulated (bold) Vs. measured(* with shield)

IX. CONCLUSION

Lumped element spice models are generated by this program for inductors and transformers which can be

used by designers to estimate inductance (L), quality factor (Q) and self-resonant frequency (SRF). New models were developed for current crowding and eddy current effects. Further work would include estimation of fringe capacitances that would give a better approximation of SRF. The inductances are more than 10 % off when there are few turns and large trace width. A better algorithm can be used to correct this and give good accuracy in all cases.

ACKNOWLEDGEMENT

The material is based on work supported by the National Science Foundation under grant ECS-9875770 with additional support from the Center for Integrated Space Microsystems, Jet Propulsion Lab.

REFERENCES

- [1] William. B. Kuhn, and Nouredin. M. Ibrahim "Approximate Analytical Modeling of Current Crowding Effects in Multi-turn Spiral Inductors," Proceedings of the 2000 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 271-274, 2000.
- [2] J. R. Long, M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors on Silicon," IEEE J. Solid-State Circuits, pp. 357-369, March 1997.
- [3] William B. Kuhn, and Naveen K. Yanduru, "Spiral Inductor Substrate Loss Modeling In Silicon RFICs" Microwave Journal , March 1999.
- [4] J. Craninckx and M.S.J. Steyaert , " A 1.8-Ghz Low-Phase Noise CMOS VCO Using Optimized Hollow Spiral Inductors, " IEEE journal of Solid-State Circuits, pp 736 – 744, May,1993.
- [5] H-S. Tsai, J. Lin, R.C.Frye, K..L. Tai, M.Y.Lau , D. Kossives, F. Hrycenko, and Y-K Chen, "Investigation of Current Crowding Effect on Spiral Inductors," IEEE MTT-S Int Topical Symp. on Technologies for Wireless Applications, pp. 139-142 , 1997.
- [6] A. M. Niknejad, and R. G. Meyer , "Analysis, Design and Optimization of Spiral Inductors and Transformers for Si RF IC's , " IEEE, Solid-State Circuits, pp 1470-1481, Oct 1998.
- [7] <http://www.eece.ksu.edu/vlsi/spiralmod>
- [8] Yorgos K. Koutsoyannopoulos, and Yannis Papananos, "Systematic Analysis and Modeling of Integrated Inductors and Transformers in RF IC Design", IEEE transactions on Circuits and Systems -II: Analog and Digital Signal Processing, vol 47, no. 8, pp 699-713, August 2000.